

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1907	PCBA,RIO,J5	J5_RIO_COMMON,EEEE:DL62
085-2805	PCBA,DEV RIO,J5	J5_RIO_DEVEL:ENG

J5 RIO BOM GROUPS

BOM GROUP	BOM OPTIONS
J5_RIO_COMMON	COMMON,ENETLOWPWR:NO,J5_RIO_PROGPARTS,HDMI_3V3_S0:YES,ALTERNATE
J5_RIO_PROGPARTS	
J5_RIO_DEVEL:ENG	ENET_ROM

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0311	128S0329		ALL	NEC alt to Sanyo
197S0450	197S0177		ALL	Alt EPSON Xtal
197S0451	197S0177		ALL	Alt NDK Xtal


Bar Code Labels / EEEE #'s

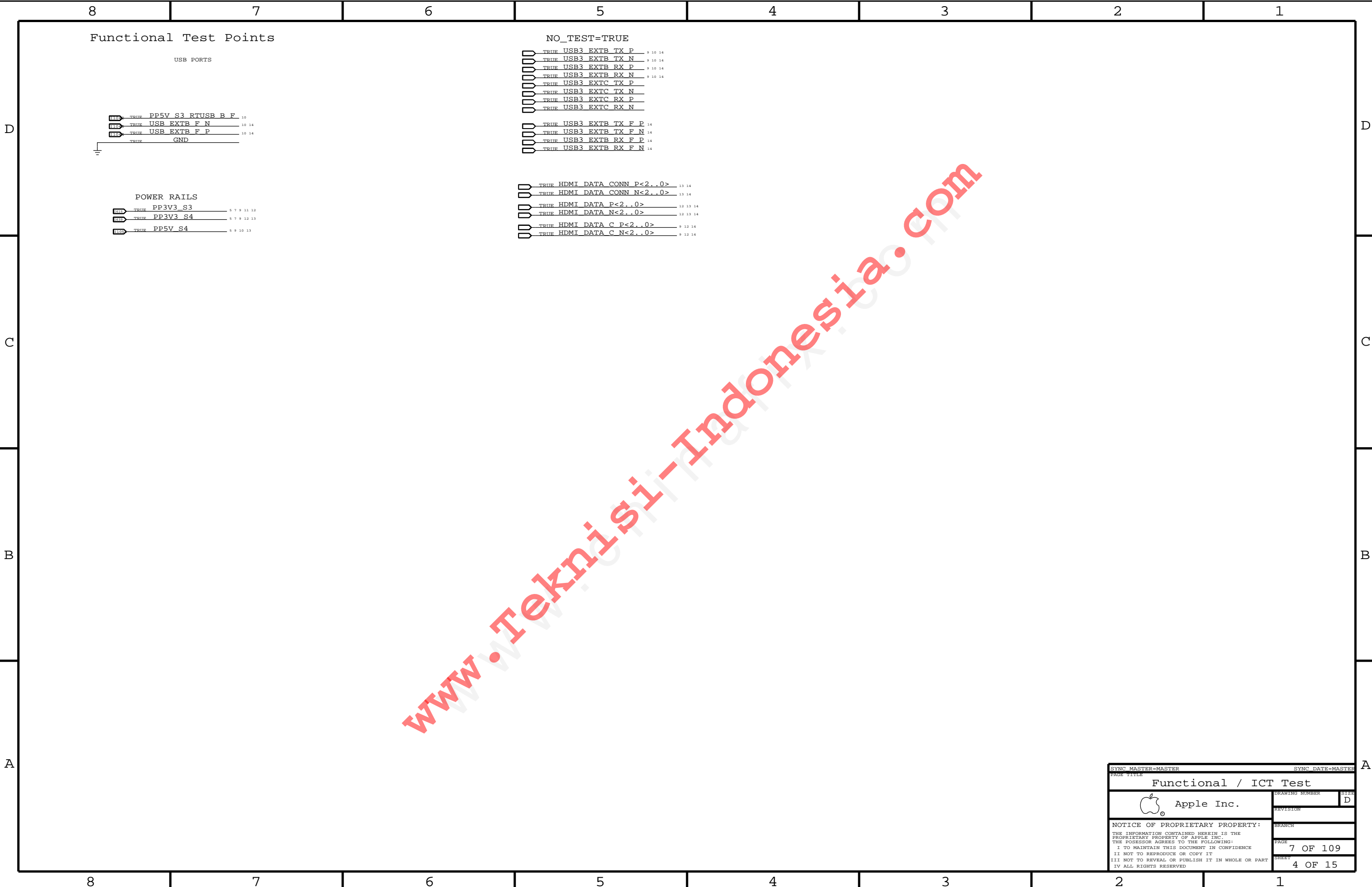
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7753	1	TEXT,LABEL,RIO,D2	[EEEE:DL62]	CRITICAL	EEEE:DL62
825-7697	1	LBL,SERIAL NO,BOARDS,D2	TEXT_LABEL	CRITICAL	EEEE:DL62

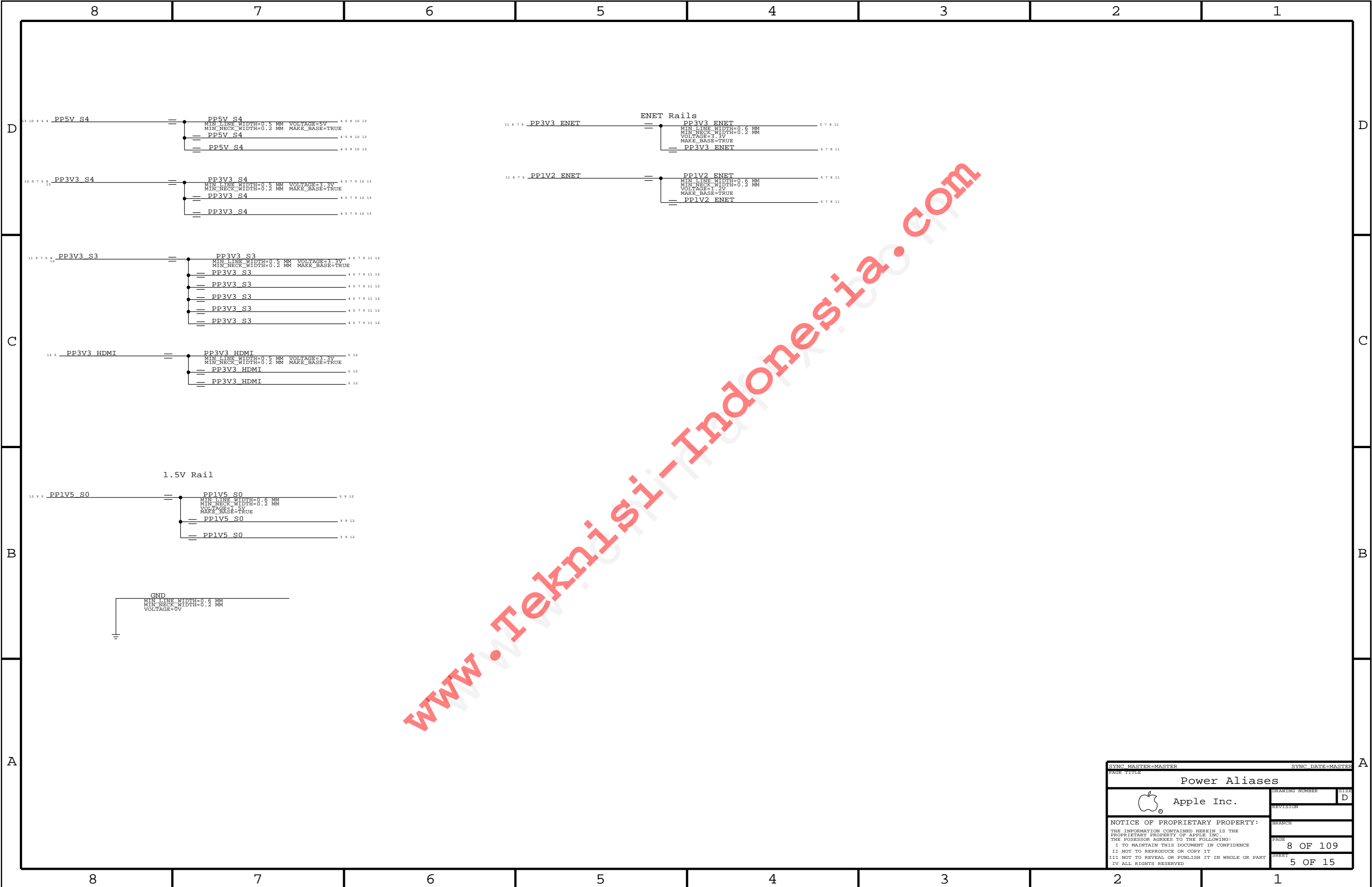
Module Parts

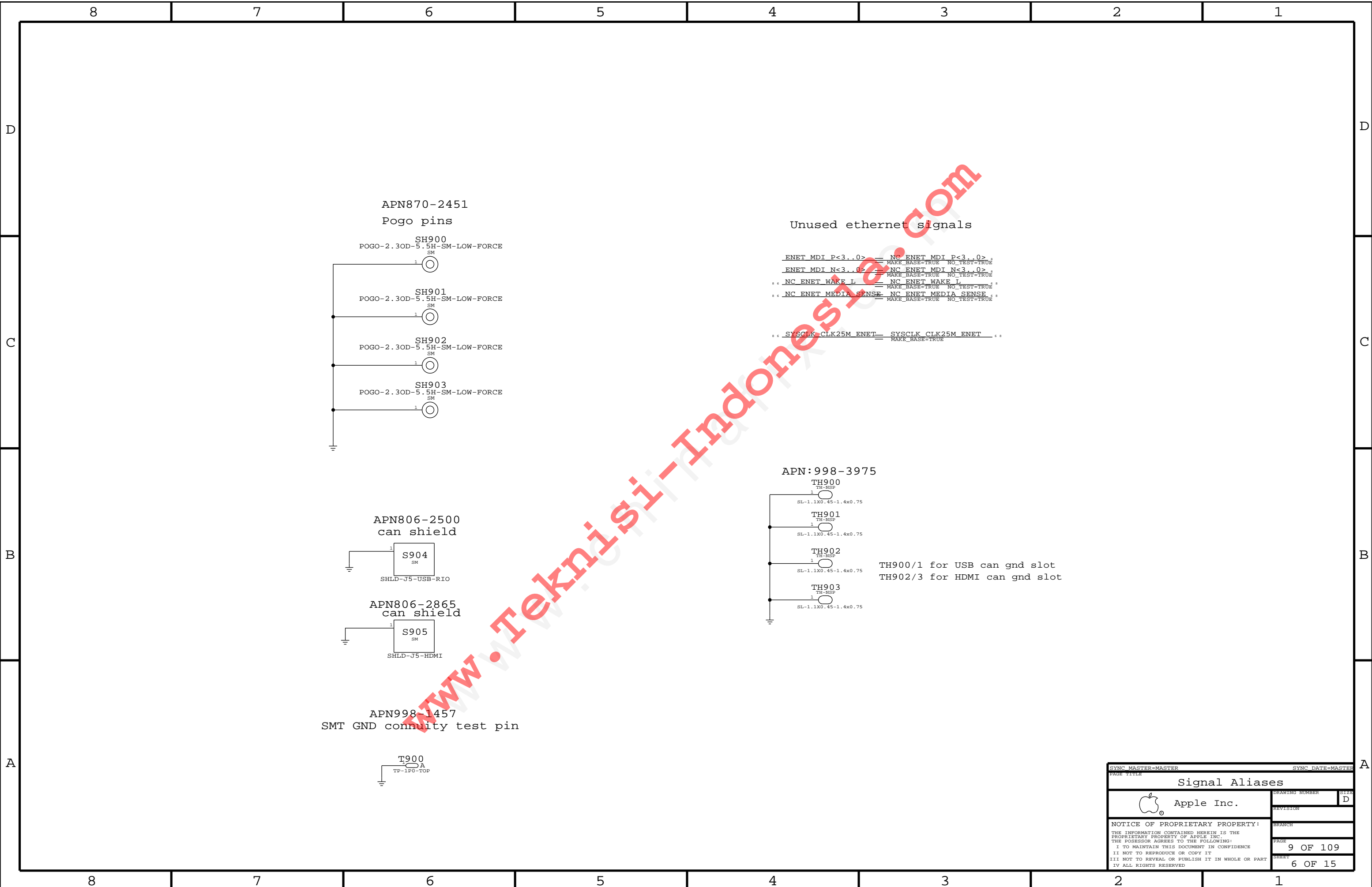
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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Programmables - All builds

SYNC MASTER-MASTER		SYNC DATE-MASTER	
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BOM Configuration			
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	REVISION		
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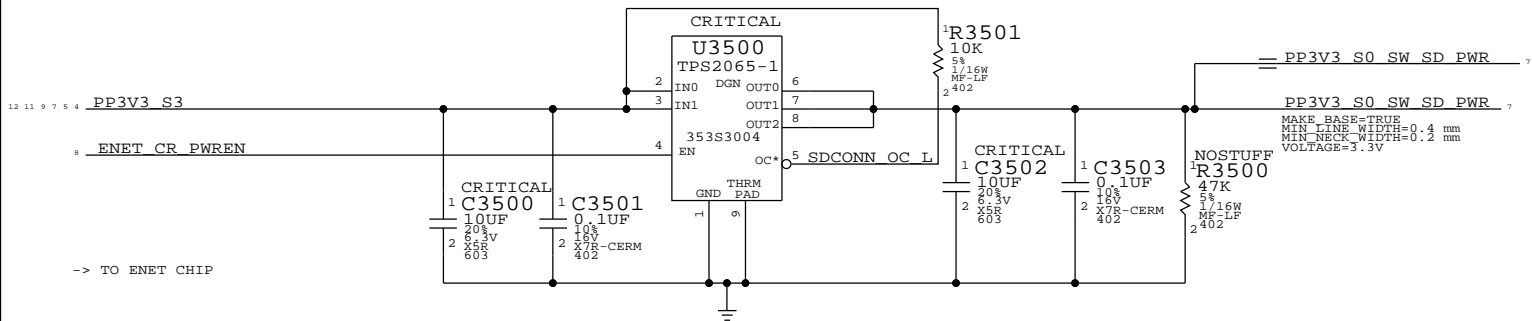
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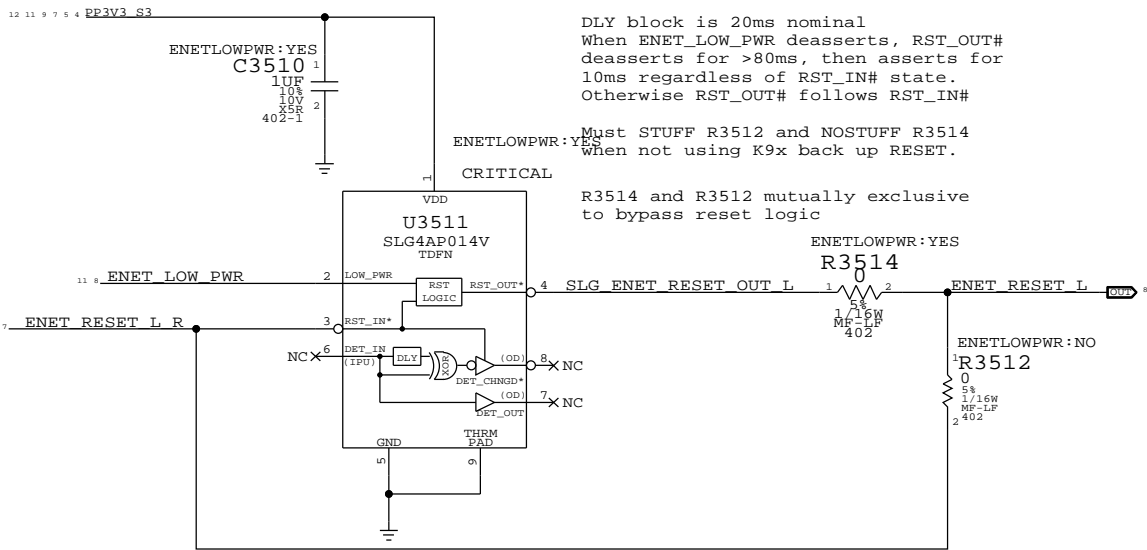
A

SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R3500 IS NOSTUFF.

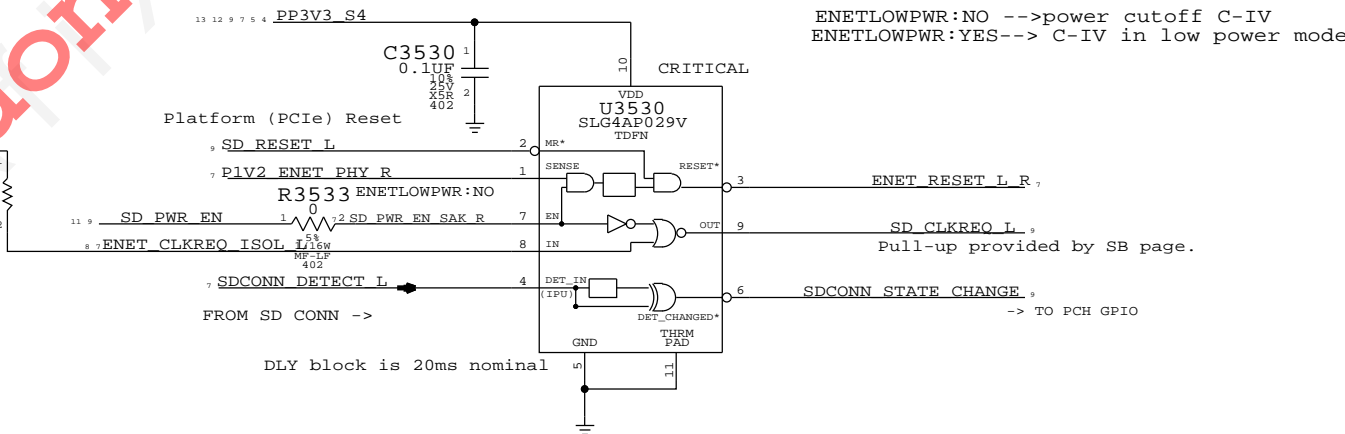


DETECT-CHANGED PCH GPIO LATCH CIRCUIT



Supervisor & CLKREQ# Isolation

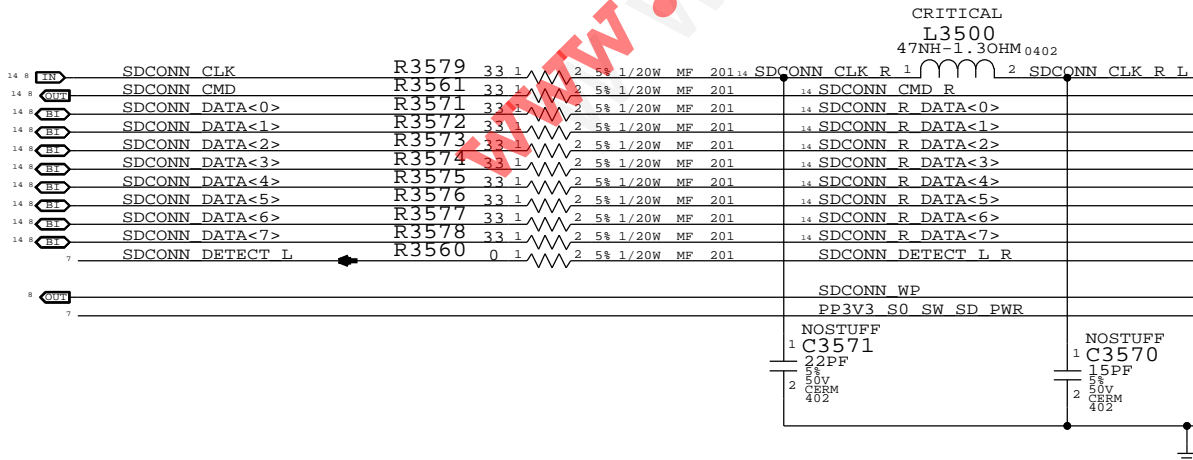
SDCONN DETECT DEBOUNCE, INVERSION, AND
DETECT-CHANGED PCH GPIO LATCH CIRCUIT



Note logic inversion of K16 connector.
Input to C-IV should remain active low

New part SLGAP029V (APN 343s0563)

SD CARD CONNECTOR

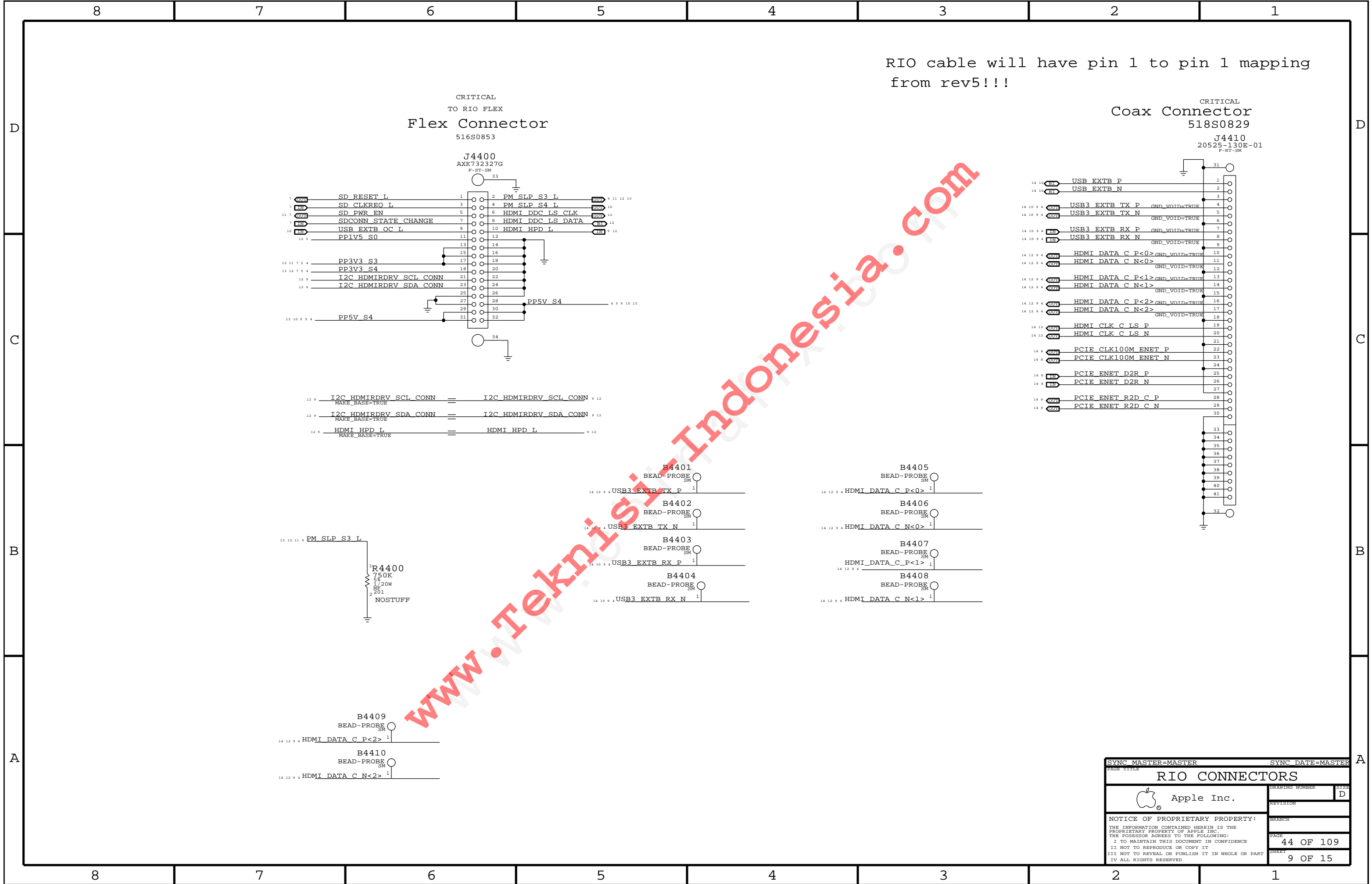


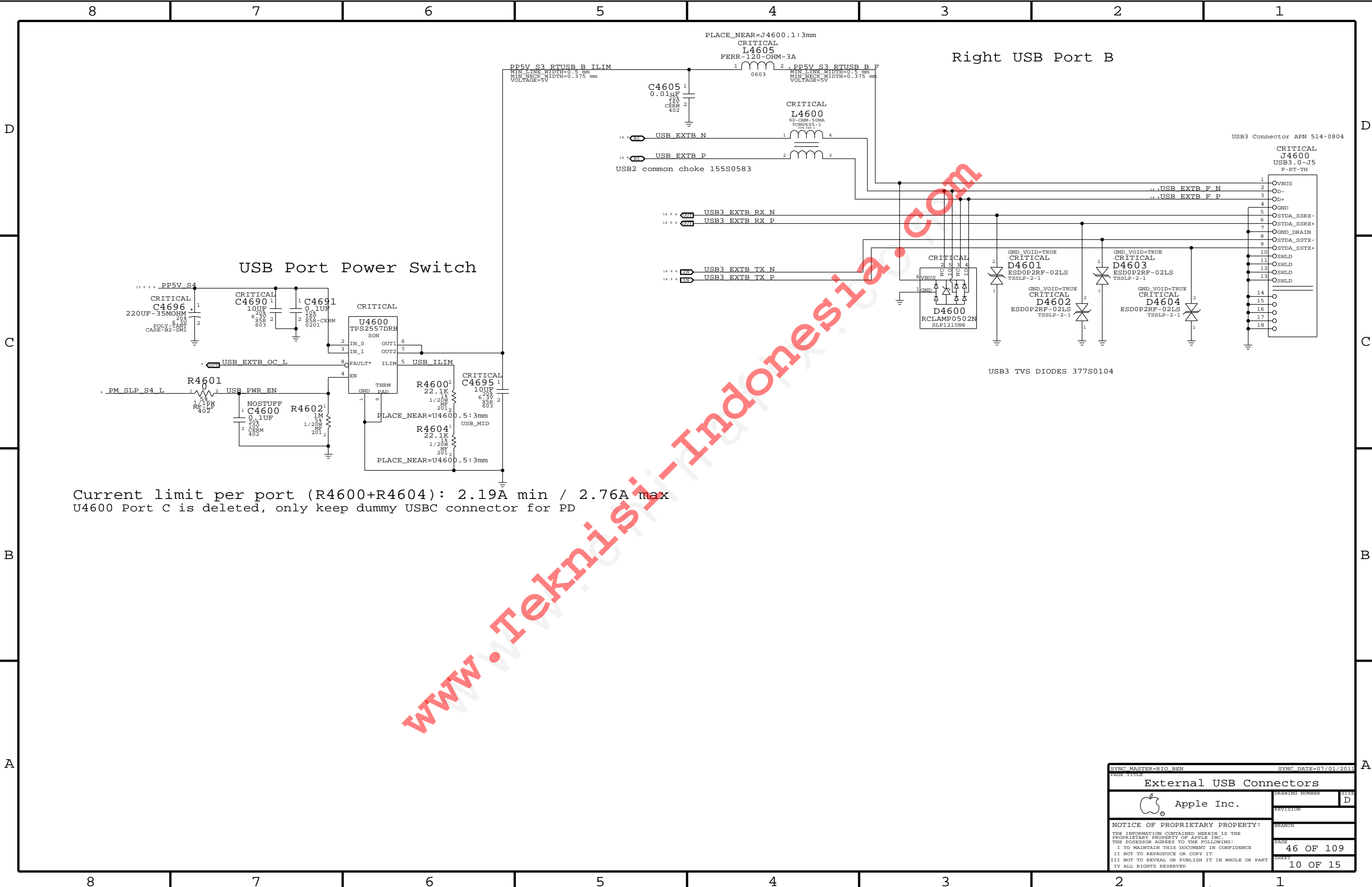
CRITICAL
516-0248
J3500
SD-CARD-J5
F-RT-TH

J5 connector different from K9X connector which was CARD INSERTED = OPEN

(CARD INSERTED = GROUND)
DAT1 CAESAR-IV CARD DETECT IS PROGRAMMABLE, BUT A SILICON BUG
MAKES THE ACTIVE-HIGH CASE UNUSABLE.

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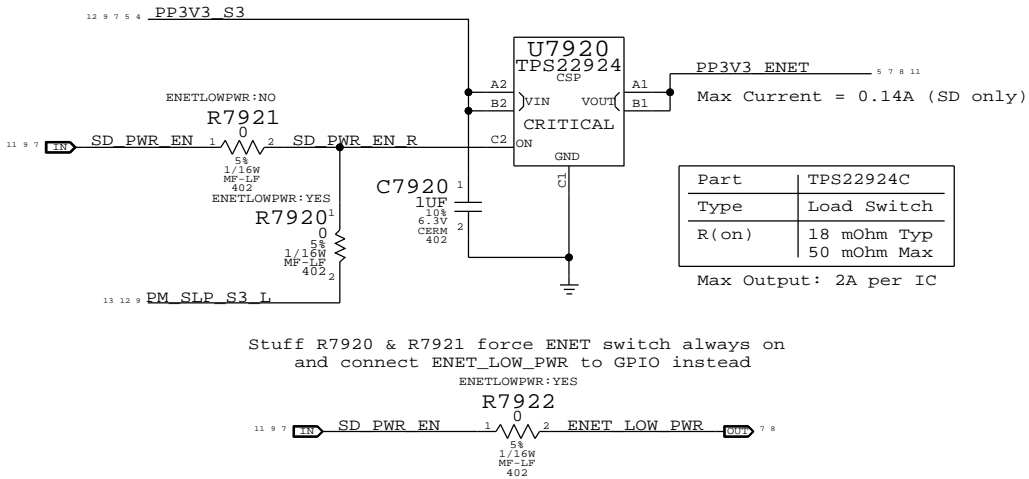




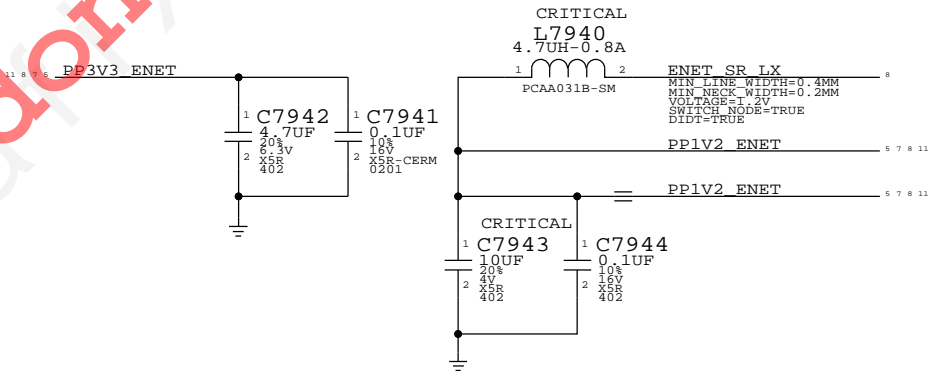
Current limit per port (R4600+R4604): 2.19A min / 2.76A max
U4600 Port C is deleted, only keep dummy USB C connector for PD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

3.3V ENET Switch

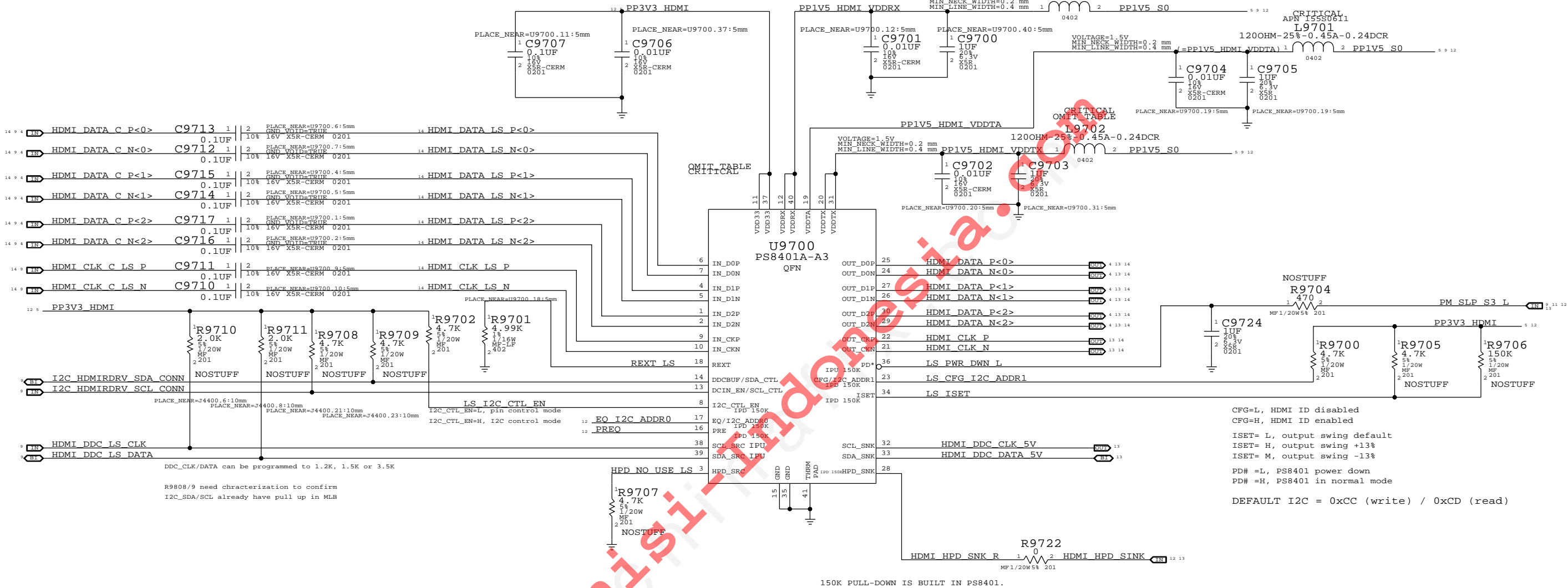


CAESAR IV 1.2V INT.VR CMPTS



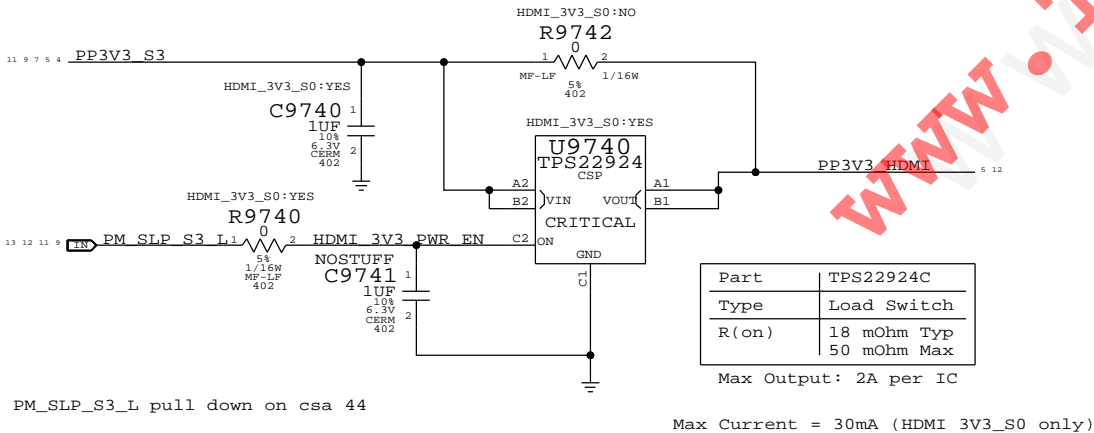
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
155S0731	2	FERR BD,60mOHM, 0402	L9700,L9702	CRITICAL	
338S1089	1	HDMI REPEATER - A3	U9700	CRITICAL	

max 1.5V current <400mA
max 3.3V current <30mA
max 1.5V_VDDRX current <180mA
max 1.5V_VDDTX current <200mA
max 1.5V_VDDTA current <20mA

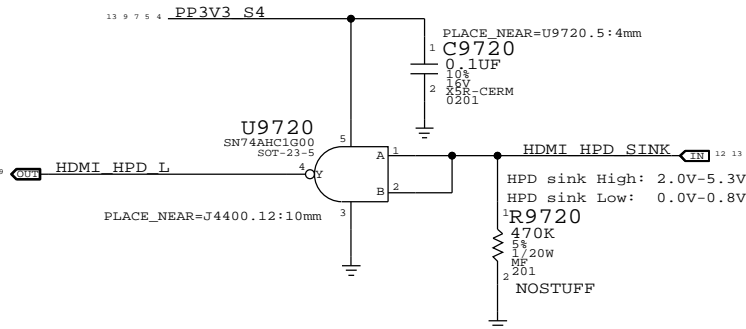


CFG=L, HDMI ID disabled
CFG=H, HDMI ID enabled
ISET= L, output swing default
ISET= H, output swing +13%
ISET= M, output swing -13%
PD# =L, PS8401 power down
PD# =H, PS8401 in normal mode
DEFAULT I2C = 0xCC (write) / 0xCD (read)

HDMI 3.3V_S0 Switch



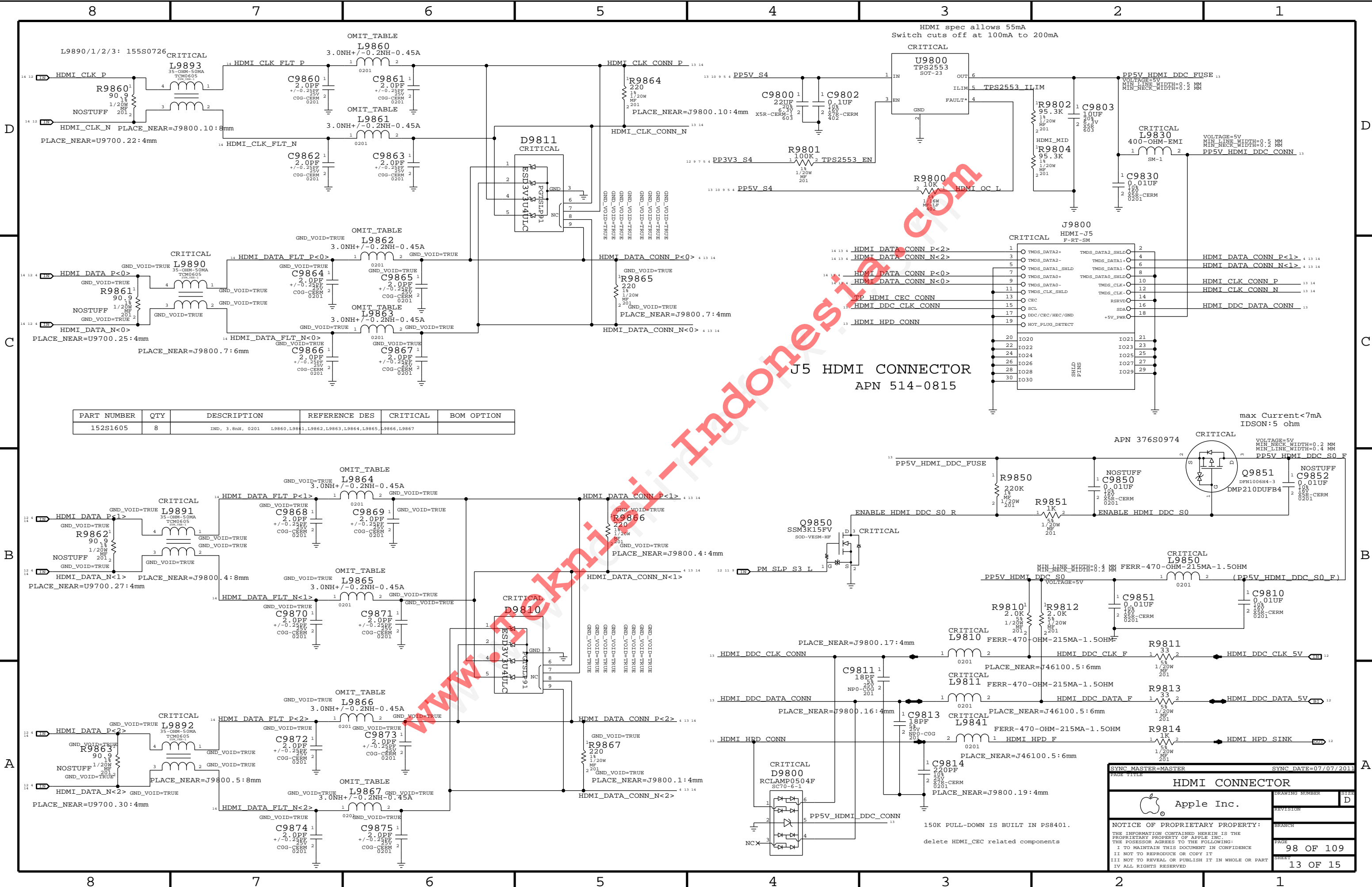
HDMI HPD 5.0V to 3.3V Level Shift



I2C control enabled when R9702 is stuffed

I2C_ADDR1	I2C_ADDR0	I2C ADDRESS(W/R)
L	L	0x4C/4D (default)
L	H	0x5C/5D
H	L	0xCC/CD
H	H	0xEC/ED

SYNC MASTER=MASTER		SYNC DATE=07/07/2011	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S1605	8	IND, 3.0nH, 0201	L9860,L9861,L9862,L9863,L9864,L9865,L9866,L9867		

SYNC MASTER=MASTER

SYNC DATE=07/07/2011

HDMI CONNECTOR

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RIO (J5) Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, BOTTOM	NO_TYPE	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.110 MM	0.110 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3	Y	0.085 MM	0.085 MM			
50_OHM_SE	ISL5, ISL6	Y	0.115 MM	0.115 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL3	Y	0.101 MM	0.101 MM		0.140 MM	0.140 MM
85_OHM_DIFF	ISL5,ISL6	Y	0.118 MM	0.118 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.130 MM	0.130 MM
90_OHM_DIFF	ISL3	Y	0.092 MM	0.092 MM		0.160 MM	0.160 MM
90_OHM_DIFF	ISL5, ISL6	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1X_DIELECTRIC	TOP, BOTTOM	0.070 MM	?
1X_DIELECTRIC	ISL3	0.120 MM	?
1X_DIELECTRIC	ISL5	0.120 MM	?
1X_DIELECTRIC	ISL6	0.120 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
3X_DIELECTRIC	ISL3, ISL5, ISL6	0.360 MM	?
4X_DIELECTRIC	ISL3, ISL5, ISL6	0.480 MM	?

HDMI_keepout should be 1.016mm. However use 0.3mm per layout restriction
HDMI_spacing should be 0.635mm. However use 0.3mm per layout restriction

NOTE: Based on RIO (J5) stackup 08/26/11.

